Instruction Manual

Tektronix

TMS 550
PowerPC MPC505 Microcontroller Support

070-9830-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

Printed in the U.S.A.

Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microcontroller Support Documentation

This instruction manual contains specific information about the TMS 550 PowerPC MPC505 microcontroller support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microcontroller support packages on the logic analyzer for which the TMS 550 PowerPC MPC505 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microcontroller support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microcontroller support packages is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to your SUT (system under test)
- Setting up the logic analyzer to acquire data from your SUT
- Acquiring and viewing disassembled data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microcontroller supports user manual.
- In the information on basic operations, the term “XXX” or “P54C” used in field selections and file names must be replaced with MPC505. This is the name of the microcontroller in field selections and file names you must use to operate the PowerPC MPC505 support.

- The term “SUT” (system under test) refers to the microcontroller-based system from which data will be acquired.
- The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.
- The term “module” refers to a 102/136-channel or a 96-channel module.
- An asterisk (*) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics and tasks:

- Support description
- Logic analyzer software compatibility and configuration
- Requirements and restrictions
- Configuring the probe adapter
- Connecting to your SUT (system under test)
- Channel assignments

Support Description

The TMS 550 microcontroller support package disassembles data from systems that are based on the Motorola PowerPC MPC505 microcontroller. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel module or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 550 microcontroller support.

The TMS 550 supports the PowerPC MPC505 microcontroller in a 160-pin QFP package.

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the following documents:

- The *PowerPC MPC505 RISC Microcontroller Technical Summary*, Motorola Inc., 1995
- The *MPC500 Family, System Interface Unit Reference Manual*, Motorola Inc., SIURM/D
- The *MPC500 Family, RCPU Reference Manual*, Motorola Inc., RCPURM/AD

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microcontroller support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the TMS 550 support, the Tektronix logic analyzer must be equipped with either a 102/136-channel module or a 96-channel module at a minimum. The module must be equipped with enough probes to acquire channel and clock data from signals in your PowerPC MPC505-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microcontroller supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your SUT, as well as the following descriptions of other PowerPC MPC505 support requirements and restrictions.

System Clock Rate. The TMS 550 support can acquire data from the PowerPC MPC505 microcontroller at speeds of up to 28 MHz[1].

ADDR11-ADDR0 Signals without a Probe Adapter. If your SUT is configured to use ADDR11-ADDR0 as address signals and not as chip select signals, you do not have to use a probe adapter.

Chip Select Signals with Internal Handshake Mode. The disassembler does not support chip select signals enabled with the internal handshake mode when the CR/DS* pin is configured as CR*. To acquire the chip select signals, the CR/DS* pin must be configured as DS*.

Little-Endian Byte Ordering. The disassembler does not support Little-Endian byte ordering.

1 **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.**

Address Pipelining. If address pipelining sustains for many sequences (approximately 1 K), there might be performance degradation when scrolling data by entering a sequence number in the Cursor field.

If address pipelining sustains for additional sequences (1 K or greater), there might be erroneous address and data association. You can use the Mark Cycles function to correct the interpretation of erroneous address and data association.

Decomposed Burst Cycles. The disassembler does not support decomposed Burst cycles when the Burst Inhibitor (BI*) signal is generated internally.

Configuring the Probe Adapter

Configuring the chip select module switch. The probe adapter has a DIP switch that must be set according to the chip select module configuration of the PowerPC MPC505. Use Table 1–1 to configure the DIP switch.

Table 1–1: Chip select DIP switch settings

Switch	Description
S1	CSBOOT*
S2	CS1*
S3	CS2*
S4	CS3*
S5	CS4*
S6	CS5*
S7	NO_CS* †
S8	Not used

† **Switch ON – If MPC505 is NOT configured for chipset operation.**
Switch OFF – If MPC505 chip select are used.

Examples of switch settings. The following example shows two possible settings:

- Example 1

  If ADDR/CS*[0-11] is to be configured without using Chip Enables the DIP switch settings would be:

  S1 – OFF (CSBOOT*)
  S2 – OFF (CS1*)
  S3 – OFF (CS2*)
  S4 – OFF (CS3*)
  S5 – OFF (CS4*)
  S6 – OFF (CS5*)
  S7 – ON (NO_CS)
  S8 – Not applicable

- Example 2

  If CSBOOT*, CS1* and CS2* are to be configured as Chip Enables the DIP switch settings would be:

  S1 – ON (CSBOOT*)
  S2 – ON (CS1*)
  S3 – ON (CS2*)
  S4 – OFF (CS3*)
  S5 – OFF (CS4*)
  S6 – OFF (CS5*)
  S7 – OFF (NO_CS)
  S8 – Not applicable

Connecting to a System Under Test

Before you connect to your SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microcontroller to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the probe adapter dimensions.

The channel and clock probes shown in this chapter are for a 102/136-channel module. The probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microcontroller supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

With a Probe Adapter

To connect the logic analyzer to a SUT using the probe adapter and test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off the logic analyzer.

CAUTION. *Static discharge can damage the microcontroller, the probe adapter, the probes, or the module. To prevent static damage, handle all the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microcontroller and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer.
3. Connect the P6434 probes to the probe adapter as shown in Figure 1–1. Match the channel groups and numbers on the probe labels to the corresponding connectors on the probe adapter.

CAUTION. *Incorrect handling of the P6434 probe while connecting it to the probe adapter can result in damage to the probe or to the mating connector on the probe adapter*

To avoid damaging the probe and probe adapter, always position the probe perpendicular to the mating connector and gently connect the probe.

4. Position the probe tip perpendicular to the mating connector and gently connect the probe as shown in Figure 1–1.
5. When connected, push down the latch releases on the probe to set the latch.

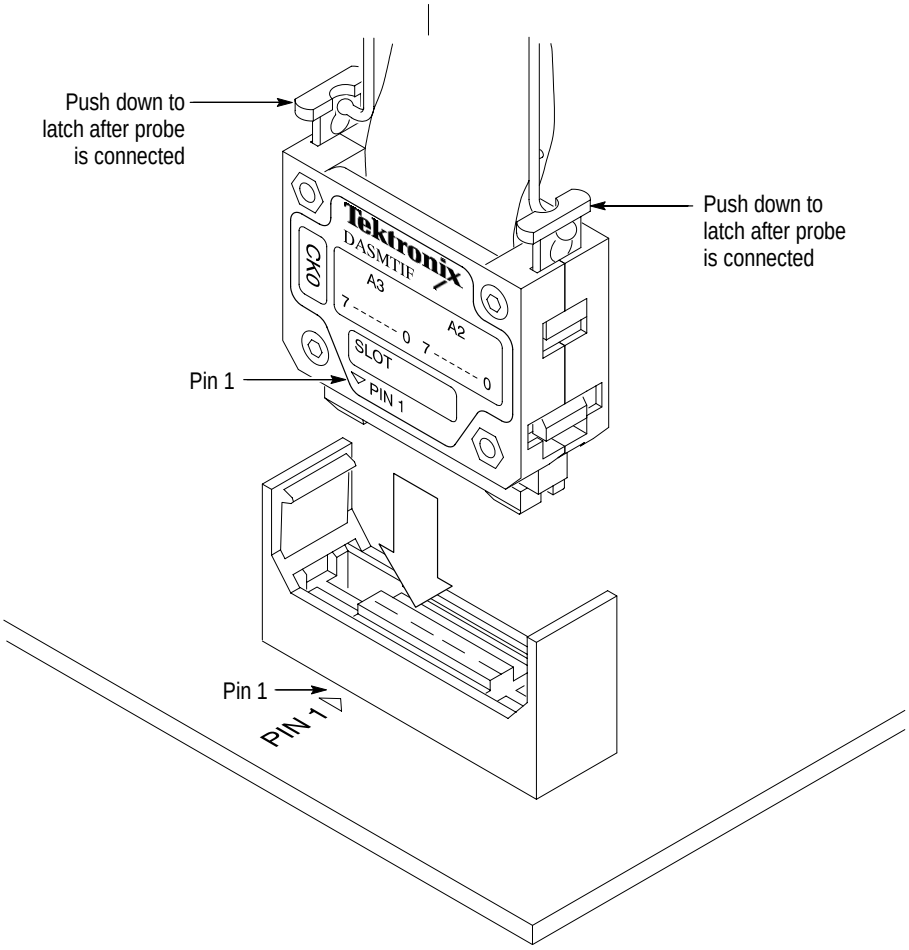


Figure 1–1: Connecting P6434 probes to the probe adapter

6. Line up the pin 1 indicator on the probe adapter circuit board (a white triangle) with the pin 1 indicator on the QFP test clip as shown in Figure 1–2.

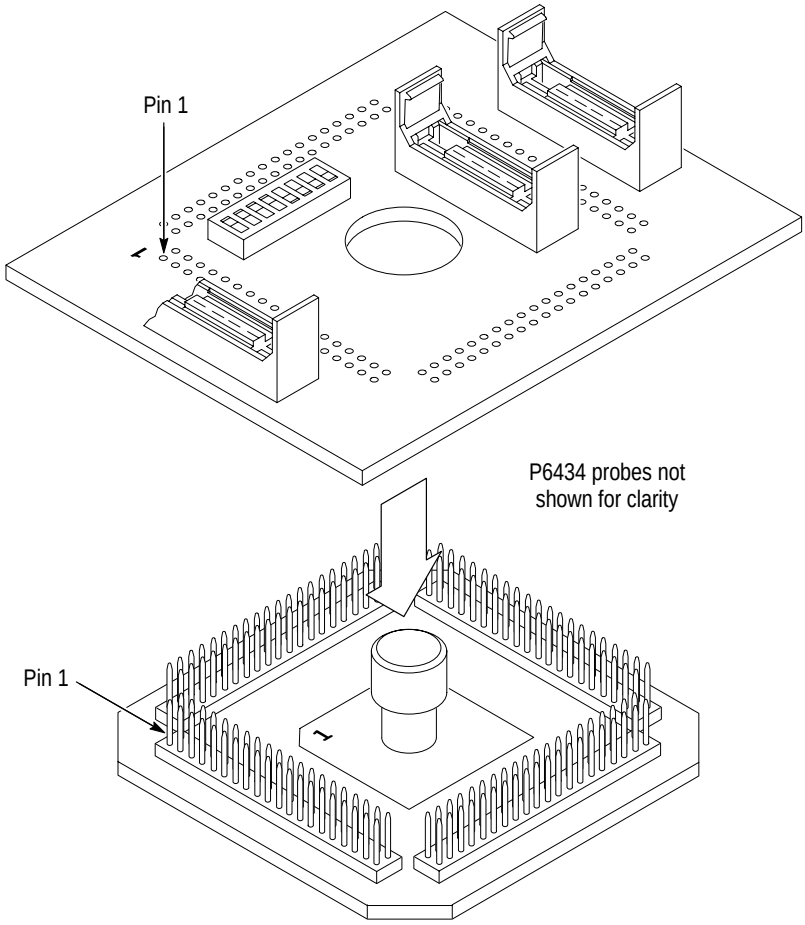


Figure 1–2: Connecting the QFP test clip to the probe adapter

7. Inspect the microcontroller on you SUT for bent or broken leads. Verify that the leads on the microcontroller are clean and free from dirt, dust, or any foreign material.

8. Inspect the pins of the QFP test clip for bent or broken contacts. Verify that the leads on the test clip are clean and free from dirt, dust or any foreign material.

9. Verify that the locking knob on the QFP test clip is not locked by turning the knob counter-clockwise.

10. Place the probe adapter onto the SUT as shown in Figure 1–3.

CAUTION. *The probe adapter board might slip off or slip to one side of the microcontroller because of the extra weight of the probes. This can damage the microcontroller and the SUT.*

To prevent this from occurring, stabilize the probe adapter by placing a non-conductive object (such as non-conductive foam) between the probe adapter and the SUT.

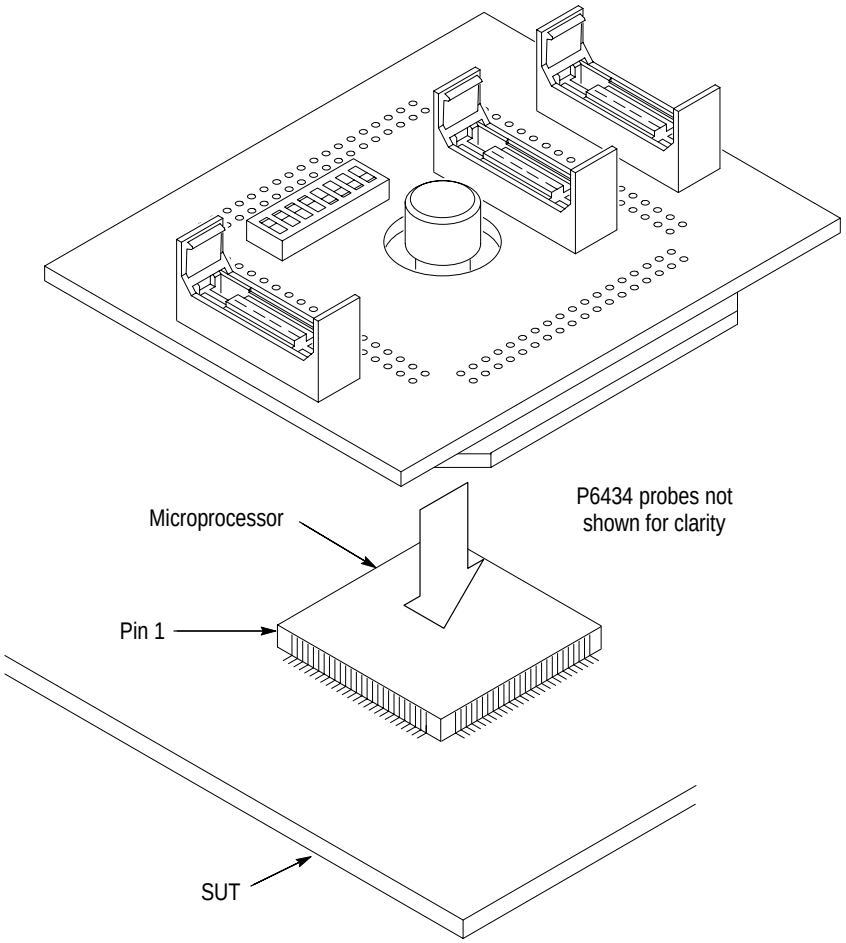


Figure 1–3: Placing the probe adapter onto the SUT

11. Lock the QFP test clip to the microcontroller by pressing down on the center locking knob and turning the locking knob clockwise.

CAUTION. *Failure to correctly place the probe adapter onto the microcontroller might permanently damage all electrical components when power is applied.*

Center the clip on the microcontroller and apply an equal downward force on all four sides of the clip. It is important to keep the QFP test clip parallel to the microcontroller to avoid damage to the SUT or QFP test clip. Do not apply leverage to the probe adapter when installing or removing it.

Removing the Probe Adapter From Your System Under Test

To remove the probe adapter from your SUT, follow these steps:

1. Unlock the QFP test clip from the microcontroller by turning the locking knob counter-clockwise.
2. Gently lift and pull the probe adapter off of the microcontroller.

Without a Probe Adapter

If the microcontroller is not configured to use chip select signals, you can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to PowerPC MPC505 signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microcontroller, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microcontroller.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.
3. Use Tables 1–2 through 1–7 to connect the channel probes to PowerPC MPC505 signal pins on the test clip or in the SUT. Channels CK:3 and C3:5 must be grounded.

   Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.
4. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the microcontroller in your SUT and attach the clip.

Alternate Microcontroller Connections

You can connect to other signals that are not required by the support so that you can analyze other signal activity in your system. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Channel Assignments

The following channel assignment tables show the probe section and channel assignments, and the signal to which each channel connects.

Channel assignments shown in Table 1–2 through Table 1–7, use the following conventions:

- All signals are required by the support unless otherwise indicated.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- An asterisk (*) following a signal name indicates an active low signal.

By default, the Address group is displayed in hexadecimal.

Refer to the *Restrictions and Requirements* description on page 1–2 for information on what the microcontroller package supports if your SUT is configured for ADDR11-ADDR0 signals or chip select signals.

Table 1–2: Address group channel assignments

Bit order	Section:channel	PowerPC MPC505 signal name
31	A3:7	ADDR0/CS0*
30	A3:6	ADDR1/CS1*
29	A3:5	ADDR2/CS2*
28	A3:4	ADDR3/CS3*
27	A3:3	ADDR4/CS4*
26	A3:2	ADDR5/CS5*
25	A3:1	ADDR6/CS6*
24	A3:0	ADDR7/CS7*

Table 1–2: Address group channel assignments (cont.)

Bit order	Section:channel	PowerPC MPC505 signal name
23	A2:7	ADDR8/CS8*
22	A2:6	ADDR9/CS9*
21	A2:5	ADDR10/CS10*
20	A2:4	ADDR11/CS11*
19	A2:3	ADDR12
18	A2:2	ADDR13
17	A2:1	ADDR14
16	A2:0	ADDR15
15	A1:7	ADDR16
14	A1:6	ADDR17
13	A1:5	ADDR18
12	A1:4	ADDR19
11	A1:3	ADDR20
10	A1:2	ADDR21
9	A1:1	ADDR22
8	A1:0	ADDR23
7	A0:7	ADDR24
6	A0:6	ADDR25
5	A0:5	ADDR26
4	A0:4	ADDR27
3	A0:3	ADDR28
2	A0:2	ADDR29
1	A0:1	Ground
0	A0:0	Ground

By default, the Data group is displayed in hexadecimal.

Table 1–3: Data group channel assignments

Bit order	Section:channel	PowerPC MPC505 signal name
31	D3:7	DATA0
30	D3:6	DATA1
29	D3:5	DATA2
28	D3:4	DATA3
27	D3:3	DATA4
26	D3:2	DATA5
25	D3:1	DATA6
24	D3:0	DATA7
23	D2:7	DATA8
22	D2:6	DATA9
21	D2:5	DATA10
20	D2:4	DATA11
19	D2:3	DATA12
18	D2:2	DATA13
17	D2:1	DATA14
16	D2:0	DATA15
15	D1:7	DATA16
14	D1:6	DATA17
13	D1:5	DATA18
12	D1:4	DATA19
11	D1:3	DATA20
10	D1:2	DATA21
9	D1:1	DATA22
8	D1:0	DATA23
7	D0:7	DATA24
6	D0:6	DATA25
5	D0:5	DATA26
4	D0:4	DATA27
3	D0:3	DATA28
2	D0:2	DATA29
1	D0:1	DATA30
0	D0:0	DATA31

By default, the Control group is displayed symbolically.

Table 1–4: Control group channel assignments

Bit order	Section:channel	PowerPC MPC505 signal name
14	C3:6	TA*
13	C3:5	CE_D*
12	C3:4	AT0*
11	C3:2	TEA*
10	C3:0	AT1*
9	C2:5	RESETOUT*
8	C2:3	TS*
7	C2:2	DS*
6	C2:1	ARETRY*
5	C1:7	CT0
4	C1:3	CT1
3	C0:7	CT2
2	C0:3	CT3
1	C0:5	WR*
0	C0:1	BURST*

By default, the ByteEnbl group is off.

Table 1–5: ByteEnbl group channel assignments

Bit order	Section:channel	PowerPC MPC505 signal name
3	C1:6	BE0*
2	C1:2	BE1*
1	C0:6	BE2*
0	C0:2	BE3*

By default, the Misc group is not visible.

Table 1–6: Misc group channel assignments

Bit order	Section:channel	PowerPC MPC505 signal name
8	C3:1	RESET* †
7	C2:7	CLKOUT †
6	C2:6	BDIP*
5	C2:4	BI*
4	C2:0	AACK*
3	C1:5	CSBOOT*
2	C1:4	BG*
1	C1:1	BR*
0	C3:7	BB*

† **Signal not required for disassembly**

The clock probes are not part of any group. The clock and other channels in this table are all used as qualifiers.

Table 1–7: Clock channel assignments

Section:channel	PowerPC MPC505 signal name
CK:3	CE_D* = ‡
CK:2	TEA* = ‡
CK:1	TA* = ‡
CK:0	CLKOUT = †
C2:3	TS* §
C2:2	DS* §
C2:1	ARETRY* §
C2:0	AACK* §

† **Signal not required for disassembly**

‡ **Clock used as a qualifier**

§ **Qualifier channel**

= Channel is doubled probed

Extra Channels

Table 1–8 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

Channels not defined in a channel group by the TMS 550 software are logged in with the Master sample point.

Table 1–8: Extra module sections and channels

Module	Section: channels
102-channels	None
136-channels	E3:7-0, E2:7-0, E1:7-0, E0:7-0, Qual:3, Qual:2
96-channels	None

Signals On The Probe Adapter But Not Acquired

The following signals are available on the probe adapter bur are not acquired by the disassembler:

DSCK	IRQ4	TRST	WP0
DSDI	IRQ5	VF0	WP1
DSDO	IRQ6	VF1	WP2
IRQ0	TCK	VF2	WP3
IRQ1	TDI	VFLS0	WP4
IRQ2	TDO	VFLS1	WP5
IRQ3	TMS		

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

The information in this section is specific to the operations and functions of the TMS 550 PowerPC MPC505 support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the PowerPC MPC505 support are:

Address, Data, Control, ByteEnbl, and Misc.

If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 1–10.

How Data is Acquired

This part of this chapter explains how the module acquires PowerPC MPC505 signals using the TMS 550 software and probe adapter. This part also provides additional information on microcontroller signals accessible on or not accessible on the probe adapter, and on extra probe channels available for you to use for additional connections.

Clocking Options

The clocking algorithm for the PowerPC MPC505 support has an additional field called “custom” that can be selected.

The TMS 550 support offers a microcontroller-specific clocking mode for the PowerPC MPC505 microcontroller. This clocking mode is the default selection whenever you load the MPC505 support.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking option for the TMS 550 support is ADDR/CS* [0-11] Pins Used As. You can acquired data from a SUT with these pins configured as chip select signals or as address bits ADDR11-ADDR0. The default selection is ChipSelects.

Custom Clocking

A special clocking program is loaded to the module every time you load the MPC505 support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the PowerPC MPC505 bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

In Custom clocking, the module clocking state machine generates one master sample for each microcontroller bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figure 2–1 shows the sample points and the master sample point for a single beat read and a burst read, in a pipelined and internal ack mode.

Figure 2–2 shows the sample points and the master sample point for a single beat read and a burst read, in non-pipelined and external ack mode.

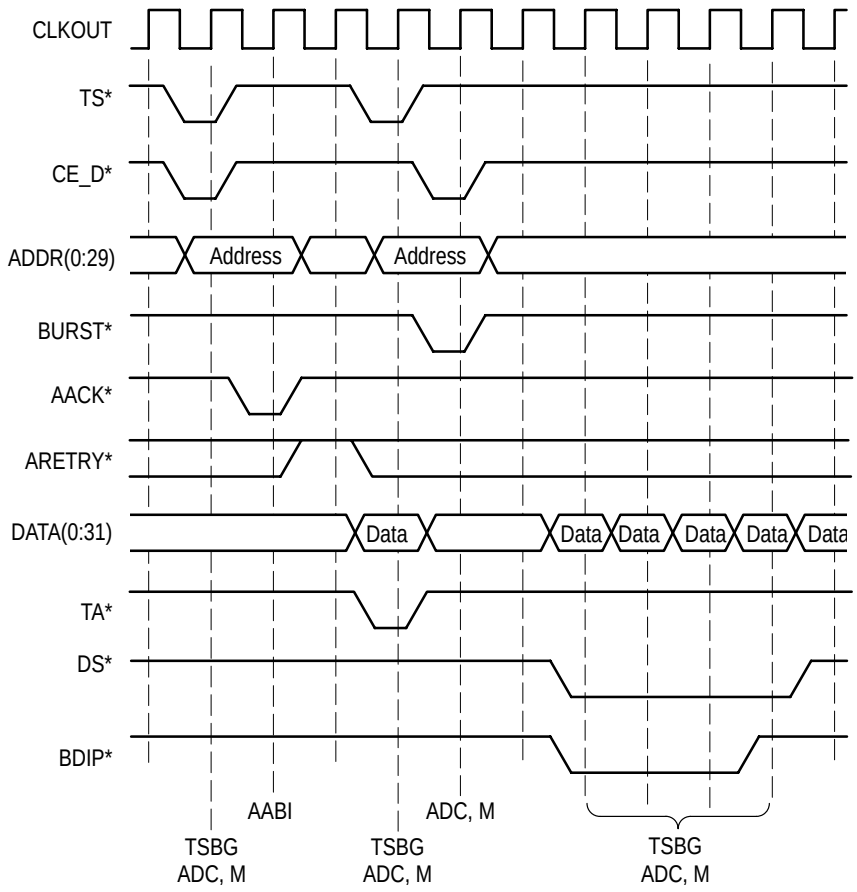


Figure 2–1: PowerPC MPC505 bus timing pipelined

***NOTE**. In figure 2–1 the burst access shown is to a region where the chip selects are configured to return acknowledgement signals TA* and AACK* internally.*

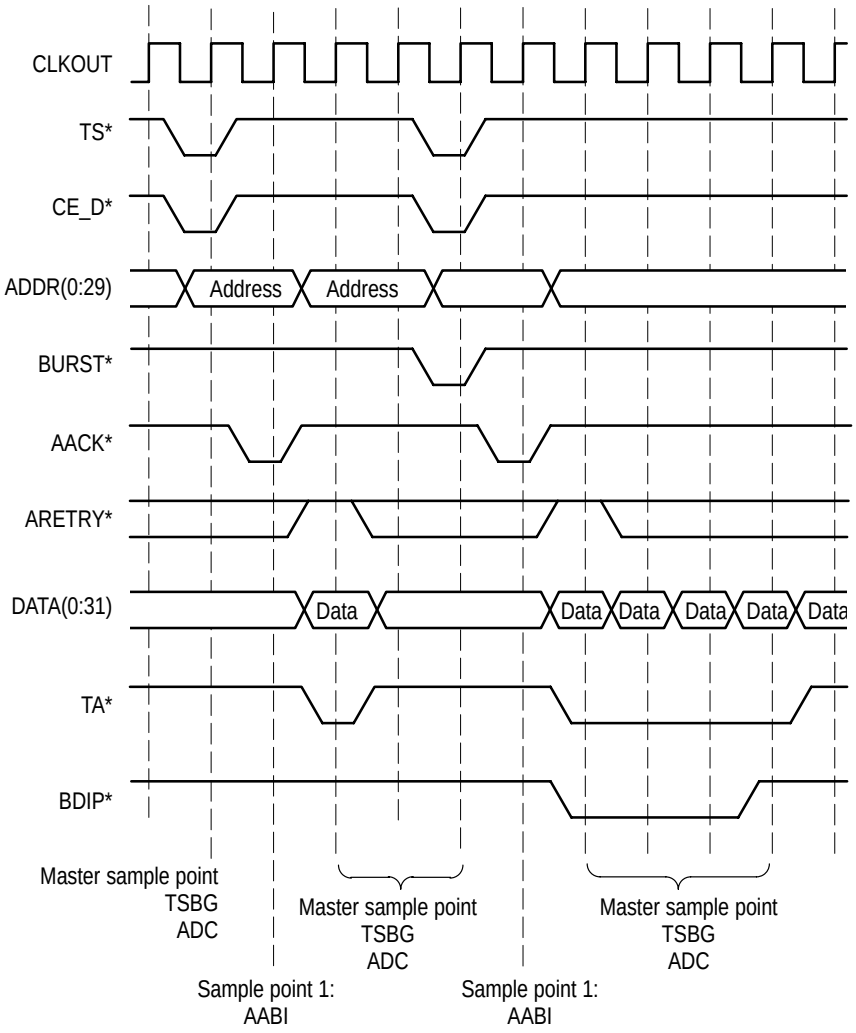


Figure 2–2: PowerPC MPC505 bus timing non-pipelined

Symbols

The TMS 550 support supplies one symbol table file. The MPC505_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file MPC505_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	Control group value TA* CE_D* AT0 TEA* AT1 RESETOUT* TS* DS* ARETRY* CT0 CT1 CT2 CT3 WR* BURST*	Meaning
Reset	X X X X X 0 X X X X X X X X X X	Processor is in reset.
Addr(Sup_Burst_Fetch) – TxError	X 0 1 0 1 1 0 X 1 0 0 0 X 1 0	Supervisor burst fetch cycle begins; previous transfer ends in error.
Addr(Sup_Burst_Read) – TxError	X 0 1 0 0 1 0 X 1 0 0 0 X 1 0	Supervisor burst read cycle begins; previous transfer ends in error.
Addr(Usr_Burst_Fetch) – TxError	X 0 0 0 1 1 0 X 1 0 0 0 X 1 0	User burst fetch cycle begins; previous transfer ends in error.
Addr(Usr_Burst_Read) – TxError	X 0 0 0 0 1 0 X 1 0 0 0 X 1 0	User burst read cycle begins; previous transfer ends in error.
Addr(Sup_Fetch) – TxError	X 0 1 0 1 1 0 X 1 0 0 0 X 1 1	Supervisor fetch cycle begins; Previous transfer ends in error.
Addr(Sup_Read) – TxError	X 0 1 0 0 1 0 X 1 0 0 0 X 1 1	Supervisor read cycle begins; previous transfer ends in error.
Addr(Sup_Write) – TxError	X 0 1 0 0 1 0 X 1 0 0 0 X 0 1	Supervisor read cycle begins; previous transfer ends in error.
Addr(Usr_Fetch) – TxError	X 0 0 0 1 1 0 X 1 0 0 0 X 1 1	User fetch cycle begins; previous transfer ends in error.
Addr(Usr_Read) – TxError	X 0 0 0 0 1 0 X 1 0 0 0 X 1 1	User read cycle begins; previous transfer ends in error.
Addr(Usr_Write) – TxError	X 0 0 0 0 1 0 X 1 0 0 0 X 0 1	User write cycle begins; Previous transfer ends in error.
Transfer Error	X X X 0 X 1 X X 1 X X X X X X X	Transfer ends in error.
Addr Retry – Data	0 X X 1 X 1 X X 0 X X X X X X X	Previous address cycle should be retried. Cycle initiated prior to that terminates.
Addr Retry – Data	X X X 1 X 1 X 0 0 X X X X X X X	Previous address cycle should be retried. Cycle initiated prior to that terminates.

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value TA* TEA* DS* CT2 CE_D* AT1 ARETRY* CT3 AT0 RESETOUT* CT0 WR* TS* CT1 BURST*	Meaning
Addr Retry	X X X 1 X 1 X X 0 X X X 0 X X X X	Previous address cycle should be retried.
Addr(Sup_Burst_Fetch) – Data	0 0 1 1 1 1 0 X 1 0 0 0 X 1 0	Supervisor burst fetch cycle begins; the previous cycle terminates.
Addr(Sup_Burst_Fetch) – Data	X 0 1 1 1 1 0 0 1 0 0 0 X 1 0	Supervisor burst fetch cycle begins; the previous cycle terminates.
Addr(Sup_Burst_Read) – Data	0 0 1 1 0 1 0 X 1 0 0 0 X 1 0	Supervisor burst read cycle begins; the previous cycle terminates.
Addr(Sup_Burst_Read) – Data	X 0 1 1 0 1 0 0 1 0 0 0 X 1 0	Supervisor burst read cycle begins; The previous cycle terminates.
Addr(Usr_Burst_Fetch) – Data	0 0 0 1 1 1 0 X 1 0 0 0 X 1 0	User burst fetch cycle begins; the previous cycle terminates.
Addr(Usr_Burst_Fetch) – Data	X 0 0 1 1 1 0 0 1 0 0 0 X 1 0	User burst fetch cycle begins; the previous cycle terminates.
Addr(Usr_Burst_Read) – Data	0 0 0 1 0 1 0 X 1 0 0 0 X 1 0	User burst read cycle begins; the previous cycle terminates.
Addr(Usr_Burst_Read) – Data	X 0 0 1 0 1 0 0 1 0 0 0 X 1 0	User burst read cycle begins; the previous cycle terminates.
Addr(Sup_Fetch) – Data	0 0 1 1 1 1 0 X 1 0 0 0 X 1 1	Supervisor fetch cycle begins; the previous cycle terminates.
Addr(Sup_Fetch) – Data	X 0 1 1 1 1 0 0 1 0 0 0 X 1 1	Supervisor fetch cycle begins; the previous cycle terminates.
Addr(Sup_Read) – Data	0 0 1 1 0 1 0 X 1 0 0 0 X 1 1	Supervisor read cycle begins; the previous cycle terminates.
Addr(Sup_Read) – Data	X 0 1 1 0 1 0 0 1 0 0 0 X 1 1	Supervisor read cycle begins; the previous cycle terminates.
Addr(Sup_Write) – Data	0 0 1 1 0 1 0 X 1 0 0 0 X 0 1	Supervisor read cycle begins; the previous cycle terminates.

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value TA* TEA* DS* CT2 CE_D* AT1 ARETRY* CT3 AT0 RESETOUT* CT0 WR* TS* CT1 BURST*	Meaning
Addr(Sup_Write) – Data	X 0 1 1 0 1 0 0 1 0 0 0 X 0 1	Supervisor read cycle begins; the previous cycle terminates.
Addr(Usr_Fetch) – Data	0 0 0 1 1 1 0 X 1 0 0 0 X 1 1	User fetch cycle begins; the previous cycle terminates.
Addr(Usr_Fetch) – Data	X 0 0 1 1 1 0 0 1 0 0 0 X 1 1	User fetch cycle begins; the previous cycle terminates.
Addr(Usr_Read) – Data	0 0 0 1 0 1 0 X 1 0 0 0 X 1 1	User read cycle begins; The previous cycle terminates.
Addr(Usr_Read) – Data	X 0 0 1 0 1 0 0 1 0 0 0 X 1 1	User read cycle begins; the previous cycle terminates.
Addr(Usr_Write) – Data	0 0 0 1 0 1 0 X 1 0 0 0 X 0 1	User write cycle begins; the previous cycle terminates.
Addr(Usr_Write) – Data	X 0 0 1 0 1 0 0 1 0 0 0 X 0 1	User write cycle begins; the previous cycle terminates.
Addr(Sup_Burst_Fetch)	1 0 1 1 1 1 0 1 1 0 0 0 X 1 0	Supervisor burst fetch cycle begins.
Addr(Sup_Burst_Read)	1 0 1 1 0 1 0 1 1 0 0 0 X 1 0	Supervisor burst read cycle begins.
Addr(Usr_Burst_Fetch)	1 0 0 1 1 1 0 1 1 0 0 0 X 1 0	User burst fetch cycle begins.
Addr(Usr_Burst_Read)	1 0 0 1 0 1 0 1 1 0 0 0 X 1 0	User burst read cycle begins.
Addr(Sup_Fetch)	1 0 1 1 1 1 0 1 1 0 0 0 X 1 1	Supervisor fetch cycle begins.
Addr(Sup_Read)	1 0 1 1 0 1 0 1 1 0 0 0 X 1 1	Supervisor read cycle begins.
Addr(Sup_Write)	1 0 1 1 0 1 0 1 1 0 0 0 X 0 1	Supervisor read cycle begins.
Addr(Usr_Fetch)	1 0 0 1 1 1 0 1 1 0 0 0 X 1 1	User fetch cycle begins.
Addr(Usr_Read)	1 0 0 1 0 1 0 1 1 0 0 0 X 1 1	User read cycle begins.
Addr(Usr_Write)	1 0 0 1 0 1 0 1 1 0 0 0 X 0 1	User write cycle begins.
Addr(Show_Cycle)	1 0 X 1 X 1 0 1 1 X X X X X X	Show cycle begins.

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value TA* TEA* DS* CT2 CE_D* AT1 ARETRY* CT3 AT0 RESETOUT* CT0 WR* TS* CT1 BURST*	Meaning
L_Mem_Access	1 X X 1 X 1 X 0 1 0 1 0 1 X X	Access to internal L–Memory.
E_Mem_Cache_Hit	1 X X 1 X 1 X 0 1 0 1 1 0 X X	Cache hit.
Int_Reg_Access	1 X X 1 X 1 X 0 1 0 1 1 1 X X	Access to an internal control register.
CSBOOT_Cache_Hit	1 X X 1 X 1 X 0 1 1 0 0 0 X X	Cache hit on access to CSBOOT region.
CS1_Cache_Hit	1 X X 1 X 1 X 0 1 1 0 0 1 X X	Cache hit on access to CS1 region.
CS2_Cache_Hit	1 X X 1 X 1 X 0 1 1 0 1 0 X X	Cache hit on access to CS2 region.
CS3_Cache_Hit	1 X X 1 X 1 X 0 1 1 0 1 1 X X	Cache hit on access to CS3 region.
CS4_Cache_Hit	1 X X 1 X 1 X 0 1 1 1 0 0 X X	Cache hit on access to CS4 region.
CS5_Cache_Hit	1 X X 1 X 1 X 0 1 1 1 0 1 X X	Cache hit on access to CS5 region.
Data	0 X X 1 X 1 X X 1 0 X X X X X	Transfer terminates.
Data	X X X 1 X 1 X 0 1 0 X X X X X	Transfer terminates.

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire and view disassembled data. The following information covers the following topics and tasks:

- Acquiring data
- Viewing disassembled data
- Changing how data is displayed

Acquiring Data

Once you load the MPC505 support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–12.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 shows these special characters and strings, and gives a definition of what they represent.

Table 2–2: Meaning of special characters in the display

Character or string displayed	Meaning
`>> or  m`	The instruction was manually marked as a program fetch
0x	Indicates the number shown is in hexadecimal

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–3 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–3: Cycle type definitions

Cycle type	Definition
(ADDR CYCLE)	Address cycle
(ADDR RETRY)	Address is to be retried
(BUS ERROR)	Error in transfer
(RESET)	Processor is in reset
(L-MEM CYCLE)	An access to an address on the internal L-bus
(CACHE HIT)	Cache hit on access to external memory
(INTERNAL REG ACCESS)	Internal register access
(CACHE HIT TO CSBOOT REGION)	Cache hit on access to CSBOOT region
(CACHE HIT TO CS1 REGION)	Cache hit on access to CS1 region
(CACHE HIT TO CS2 REGION)	Cache hit on access to CS2 region
(CACHE HIT TO CS3 REGION)	Cache hit on access to CS3 region
(CACHE HIT TO CS4 REGION)	Cache hit on access to CS4 region
(CACHE HIT TO CS5 REGION)	Cache hit on access to CS5 region
(SUP DATA READ) §	Supervisor data read cycle
(USR DATA READ) §	User data read cycle
(SUP DATA WRITE) §	Supervisor data write cycle
(USR DATA WRITE) §	User data write cycle
(CACHE FILL) §	Burst read transfer that takes place after wrap around at the end of cache line
(INCOMPLETE DATA) §	Data with corresponding address unacquired
(INCOMPLETE ADDR) §	Address with corresponding data unacquired
(RESV. START) §	Reservation cycle caused by a lwarx instruction
(FLUSH) §	Cycle was fetched but not executed
(EXTENSION) §	Cycle is an extension to a preceding instruction opcode
(UNKNOWN) §	Combination of control bits is unexpected or unrecognized

§ **Computed cycle types.**

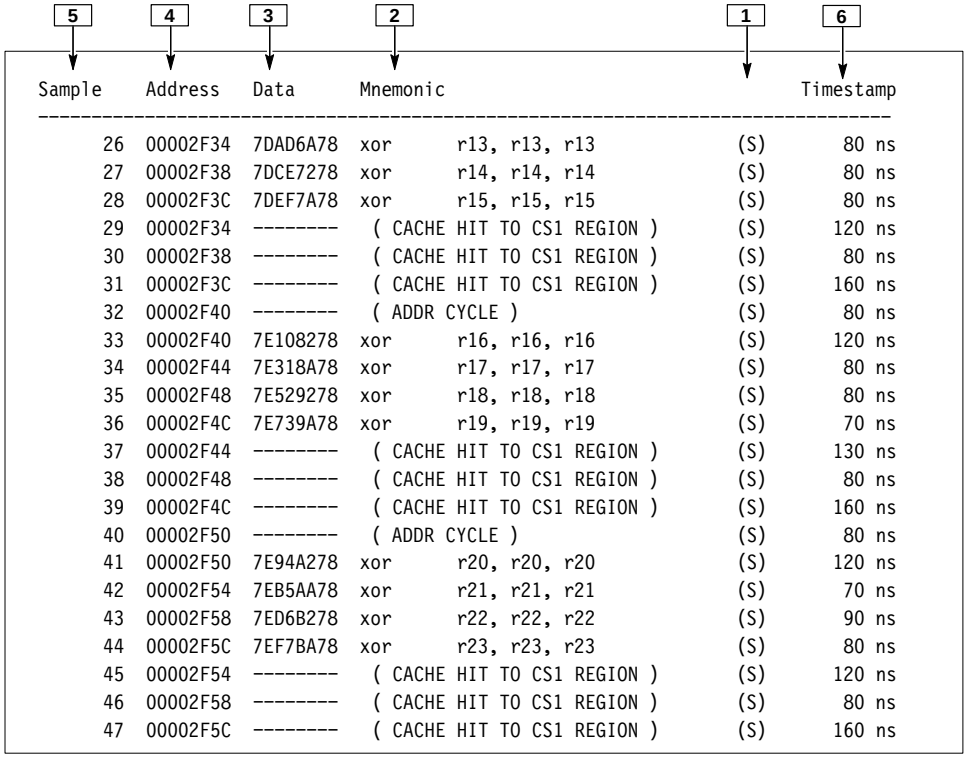


Figure 2–3: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the PowerPC MPC505 address bus.

3 **Data Group.** Lists data from channels connected to the PowerPC MPC505 data bus.

4 **Mnemonics Column.** Lists the disassembled instructions and cycle types.

5 **Control Group.** Lists data from channels connected to PowerPC MPC505 microcontroller control signals (shown symbolically).

6 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the PowerPC MPC505 microcontroller are as follows:

b	bl	rfi
ba	bla	sc

Instructions that may generate a change in the flow of control in the PowerPC MPC505 microcontroller are as follows:

bc	bca	bcl	bcla
bclr	bclrl	bcctr	bcctrl
tw	twi		

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the PowerPC MPC505 microcontroller are as follows:

sc	rfi

Instructions that might generate a subroutine call or a return in the PowerPC MPC505 microcontroller are as follows:

tw	twi

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the PowerPC MPC505 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

There are no optional fields for this support package. Refer to the information on basic operations for descriptions of common fields.

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

- Specify the starting address of the exception vector table
- Specify the Burst protocol
- Select the Block Size, Base Address, and Port size
- Specify the SUT configuration

Exception Prefix. You can select the starting address of the exception table using the following selections:

0x00000000 (default setting)
0xFFF00000

Burst Timing. Two burst timing protocols are available:

BDIP* (default setting)
LAST*

Chip Selects. Pins ADDR/CS[0-11]* can be configured as either address bits or chip selects. The two chip select settings available are:

Enabled (default setting)
Disabled

If you set Chip Selects to Enabled, you must choose the Block Size, Base Address and Port Size.

If any of the pins CS[1-5]* is not configured as a Chip Enable for a Main Block, set the corresponding Block Size field to zero (0).

Block Size. Block Size (CS[1-5]*) is a six digit hexadecimal fill-in field. Set the Block Size according to Table 2–4.

Table 2–4: Block Size

Block size (BlkSize)	Value of digit
Not a Chip Enable of a Main Block	0
4K	1
8K	2
16K	3
32K	4
64K	5
128K	6

Table 2–4: Block Size (cont.)

Block size (BlkSize)	Value of digit
256K	7
512K	8
1M	9
2M	a
4M	b
8M	c
16M	d
32M	e
64M	f

CSBOOT* Base Address. This is a 32-bit fill in field. Enter the base address of the region controlled by the CSBOOT Chip Enable.

CS1* Base Address. This is a 32-bit fill in field. Enter the base address of the region controlled by the CS1* Chip Enable.

CS2* Base Address. This is a 32-bit fill in field. Enter the base address of the region controlled by the CS2* Chip Enable.

CS3* Base Address. This is a 32-bit fill in field. Enter the base address of the region controlled by the CS3* Chip Enable.

CS4* Base Address. This is a 32-bit fill in field. Enter the base address of the region controlled by the CS4* Chip Enable.

CS5* Base Address. This is a 32-bit fill in field. Enter the base address of the region controlled by the CS5* Chip Enable.

Port Size. This is a 6-bit fill-in field. Set the Block Size according to Table 2–5 and Table 2–6.

Table 2–5: Bit Significance

Bit significance	Description
Most Significant Bit	CSBOOT*
	CS1*
	CS2*
	CS3*
	CS4*
Least Significant Bit	CS5*

Table 2–6: Port Size

Port Size	Value of digit
32 bit	1
16 bit	0

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it.

The Marking options allowed on data sequences where the associated address signals a fetch are:

Opcode – Mark cycle as an instruction opcode

Extension – Mark cycle as an extension to an instruction opcode (Only for 16-bit port accesses)

Flush – Mark cycle as a flushed cycle

The following marking options are allowed on all data sequences:

Incomplete Data – Do not associate this data cycle with any address cycle

The following marking options are available for associated sequences having address cycles:

Incomplete Addr – Do not associate this data cycle with any address cycle

The following marking options are allowed on all sequences:

Undo mark – Remove all marks from the current sequence

Displaying Exception Vectors

The disassembler can display exception vectors.

You can relocate the table by selecting the starting address in the Exception Prefex field.

You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

Table 2–7 lists the PowerPC MPC505 interrupt and exception vectors.

Table 2–7: Interrupt and exception vectors

Location in Exception Vector table (in hexadecimal)	Displayed exception name
00000	(RESERVED EXCEPTION)
00100	(SYSTEM RESET EXCEPTION)
00200	(MACHINE CHECK EXCEPTION)
00300	(DATA ACCESS EXCEPTION)
00400	(INSTRUCTION ACCESS EXCEPTION)
00500	(EXTERNAL INTERRUPT EXCEPTION)
00600	(ALIGNMENT EXCEPTION)
00700	(PROGRAM EXCEPTION)
00800	(FLOATING-POINT UNAVAILABLE EXCEPTION)
00900	(DECREMENTER EXCEPTION)
00A00	(RESERVED EXCEPTION)
00B00	(RESERVED EXCEPTION)
00C00	(SYSTEM CALL EXCEPTION)
00D00	(TRACE EXCEPTION)
00E00	(FLOATING-POINT ASSIST EXCEPTION)
01000	(SOFTWARE EMULATION EXCEPTION)
01C00	(DATA BREAKPOINT EXCEPTION)
01D00	(INSTRUCTION BREAKPOINT EXCEPTION)
01E00	(MASKABLE EXT BREAKPOINT EXCEPTION)
01F00	(NONMASKABLE EXT BREAKPOINT EXCEPTION)

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your PowerPC MPC505 microcontroller bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Certification and compliance table
- Dimensions

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microcontroller in its own operating environment with little effect on that system.

The probe adapter consists of a circuit board and a QFP IC test clip for a PowerPC MPC505 microcontroller. The probe adapter connects to the microcontroller on your SUT. Signals from the microcontroller-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the SUT.

The probe adapter accommodates the Motorola PowerPC MPC505 microcontroller in a 160-pin QFP package.

Specification Tables

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–1 shows the electrical requirements the SUT must produce for the support to acquire correct data. Table 3–2 shows the environmental specifications. Table 3–3 shows the certifications and compliances that apply to the probe adapter.

NOTE. *In Table 3–1, for the 102/136-channel module the electrical loading on one podlet is 20 kΩ in parallel with 2 pF.*

For the 96-channel module the electrical loading on one podlet is 100 kΩ in parallel with 10 pF.

Table 3–1: Electrical specifications

Characteristics	Requirements	
SUT DC power requirements		
Voltage	3.3 Vdc ± 0.3 Vdc	
Current	I max (calculated) 80 mA	
SUT clock rate	Max. 28 MHz	
Minimum setup time required, all signals	5 ns	
Minimum hold time required, all signals	0 ns	
	Specification	
Measured typical SUT signal loading	**AC load**	**DC load**
TEA*, TA*, CLKOUT	19 pF + 2 podlets	2 podlets
CSBOOT*, CS1*-CS5*	74 nF + 1 podlet	1 PALLV22V10 + 1 podlet
ADDR6-ADDR29, ADDR0, DATA0-DATA31, TS*, AACK*, ARETRY*. DS*, AT0*, AT1*, WR*, BURST*, BI*, BDIP*, BG*, BE3*-BE0*, CT3-CT0, BR*, BB*, RESET*, RESETOUT*	24 pF + 1 podlet	1 podlet

Table 3–2: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

*** Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed PowerPC MPC505 microcontroller thermal considerations. Forced air cooling might be required across the CPU.**

Table 3–3: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.

Figure 3–1 shows the dimensions of the probe adapter. Figure 3–2 shows the dimensions of the test clip. Figure 3–3 shows the minimum vertical clearance of the probe adapter and test clip. Figure 3–4 shows the height of the P6434 probes after they are connected to the probe adapter.

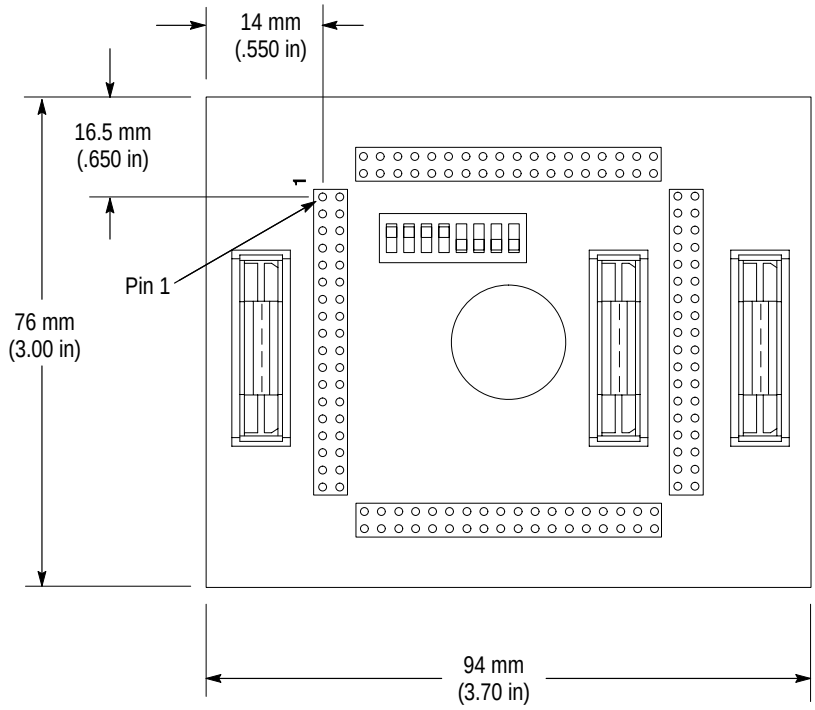


Figure 3–1: Dimensions of the probe adapter

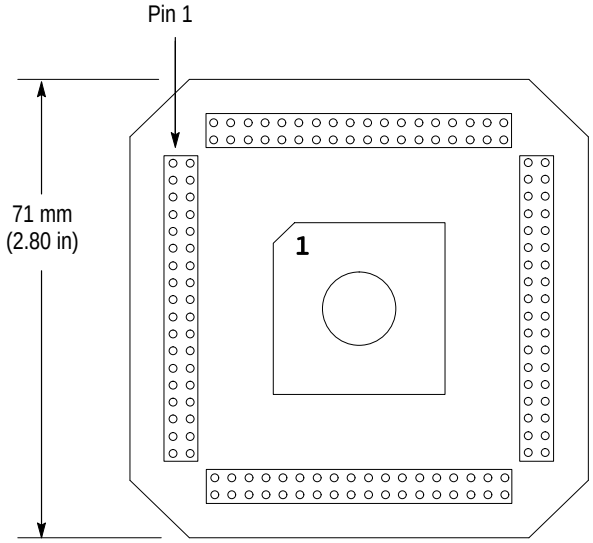


Figure 3–2: Dimensions of the test clip

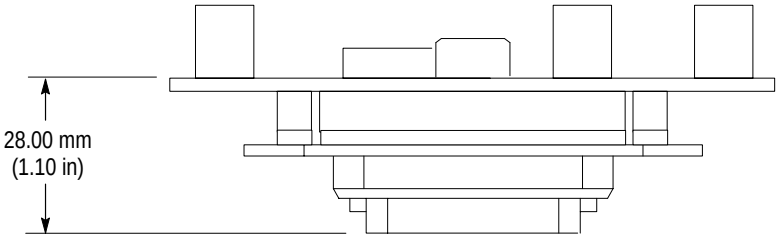


Figure 3–3: Vertical height of the probe adapter and test clip

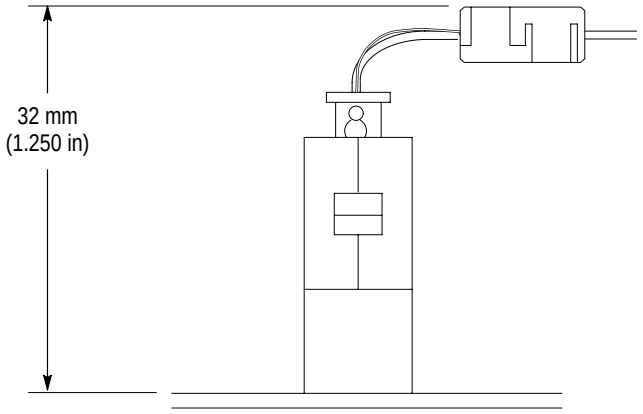


Figure 3–4: Height of the P6434 probe after connected to the probe adapter

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

Probe Adapter Circuit Description

The PowerPC MPC505 support probe adapter is a nonintrusive circuit board that interfaces between the microcontroller on your SUT and the logic analyzer. The probe adapter is a two part system that is made up of a circuit board and a EIAJ locking QFP test clip. Refer to *Getting Started* in this manual for more information on connecting the probe adapter to your SUT.

The probe adapter has three MICTOR connectors marked C, A, and D, for control, address, and data, respectfully. The three MICTOR connector interface the probe adapter to the logic analyzer by using P6434 probes.

There is one eight position DIP switch that is used to configure the chip select and address lines. Only the first seven switches are used, the eighth switch is not connected. Refer to *Getting Started* in this manual for more information on configuring the DIP switch.

The probe adapter has one low voltage 22V10 PAL that is used to synthesize CE_D* from the chip selects CS[1-5]*, CSBOOT* and NO_CS signals. Signal NO_CS is a derived signal.

Attached to the probe adapter is a EIAJ locking QFP test clip. The EIAJ locking QFP test clip makes the connection between the probe adapter and the microcontroller on your SUT.

Inspection and Cleaning

The EIAJ locking QFP test clip needs to be carefully inspected before it is used. Inspect the EIAJ locking QFP test clip for foreign matter between the contacts or bent or broken contacts. Clean the EIAJ locking QFP test clip with a clean soft dust brush or low velocity compressed air. Foreign matter may be removed from between the contacts with a fine tip tweezer.

CAUTION. *Do not clean the probe adapter or the EIAJ locking QFP test clip with chemicals, liquids, or abrasive cleaners.*

Do not submerse the probe adapter in any fluid as the DIP switch is not sealed. Subjecting the DIP switch to liquids will cause shorting and may damage the probe adapter, your microcontroller, and your SUT.

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 550 PowerPC MPC505 microcontroller support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

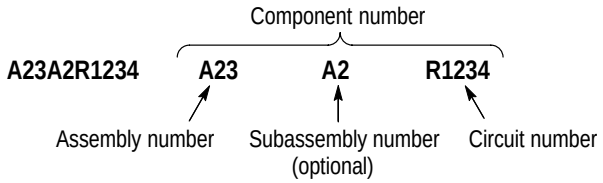
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
05276	ITT POMONA ELECTRONICS	1500 E NINTH ST	POMONA, CA 91766–3835
09353	C & K COMPONENTS CORP	15 RIVERDALE AVENUE	NEWTON, MA 02158
53387	3M COMPANY	ELECTRONICS PRODUCTS DIV 3M AUSTIN CENTER	AUSTIN, TX 78769–2963
60381	PRECISION INTERCONNECT CORP.	16640 SW 72ND AVE	PORTLAND, OR 97224
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01	010–0611–00			PROBE ADAPTER: MPC505, QFP, 160–PIN, PROBE ADAPTER, TMS550	80009	010–0611–00
A01	103–0408–00			ADAPTER, QFP: ADAPTER, QFP, 160 POS, 0.65MM CTR, EIAJ QFP TO 0.25 SQ, 2X20 HDRS, TEST CLIP, 31.2MM L	05276	5645L–2
A01	671–4079–00			CIRCUIT BD ASSY: MPC505, QFP–160, SOLDERED, 389–2384–00 WIRED, TMS550 OPT 01	80009	671–4079–00
A01J200	131–6134–01			CONN, PLUG: SMD, MICTOR, PCB, FEMALE, STR, 38 POS, 0.025 CTR, 0.245 H, GOLD	00779	767004–1
A01J210	131–5132–00			CONN, BOX: PCB, BOTTOM ENTRY, FEMALE, STR, 2 X 20, 0.1 CTR, 0.235 H X 0.130 TAIL, 10 GOLD, DUAL ENT	53387	961873–01–20–10
A01S100	260–5000–00			SWITCH, SLIDE: SPST, DIP8 POSITION, GOLD OVER NICKEL, 3A, 2PF, SEALED, 90HBW08S, 44MM T&R	09353	LD08HOSK1
A01X1J200	105–1089–00			LATCH ASSY: LATCH HOUSING ASSY, VERTICAL MOUNT, 2/PKG, 0.48 H X 1.24 L, W/PCB SINGLE CLIP, PEPPER	60381	105–1089–00

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 550 PowerPC MPC505 microcontroller support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
05276	ITT POMONA ELECTRONICS	1500 E NINTH ST	POMONA, CA 91766–3835
09353	C & K COMPONENTS CORP	15 RIVERDALE AVENUE	NEWTON, MA 02158
53387	3M COMPANY	ELECTRONICS PRODUCTS DIV 3M AUSTIN CENTER	AUSTIN, TX 78769–2963
60381	PRECISION INTERCONNECT CORP.	16640 SW 72ND AVE	PORTLAND, OR 97224
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010–0611–00			1	PROBE ADAPTER: MPC505, QFP, 160-PIN, PROBE ADAPTER, TMS550	80009	010–0611–00
–1	105–1089–00			3	LATCH ASSY: LATCH HOUSING ASSY, VERTICAL MOUNT, 2/PKG, 0.48 H X 1.24 L, W/PCB SINGLE CLIP, PEPPER	60381	105–1089–00
–2	131–6134–01			3	CONN, PLUG: SMD, MICTOR, PCB, FEMALE, STR, 38 POS, 0.025 CTR, 0.245 H, GOLD	00779	767004–1
–3	671–4079–00			1	CIRCUIT BD ASSY: MPC505, QFP-160, SOLDERED, 389–2384–00 WIRED, TMS550 OPT 01	80009	671–4079–00
–4	131–5132–00			4	CONN, BOX: PCB, BOTTOM ENTRY, FEMALE, STR, 2 X 20, 0.1 CTR, 0.235 H X 0.130 TAIL, 10 GOLD, DUAL ENT	53387	961873–01–20–10
–5	103–0408–00			1	ADAPTER, QFP: ADAPTER, QFP, 160 POS, 0.65MM CTR, EIAJ QFP TO 0.25 SQ, 2X20 HDRS, TEST CLIP, 31.2MM L	05276	5645L–2
–6	260–5000–00			1	SWITCH, SLIDE:SPST,DIP8 POSITION,GOLD OVER NICKEL, 3A, 2PF, SEALED, 90HBW08S, 44MM T&R	09353	LD08HOSK1
					STANDARD ACCESSORIES		
	070–9830–00			1	MANUAL, TECH: INSTRUCTION, MPC505, DISSASEMBLER, TMS 550	80009	070–9830–00
	070–9803–00			1	MANUAL, TECH: TLA 700 SERIES MICROPROCESSOR SUPPORT INSTALLATION	80009	070–9803–00
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH: BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00

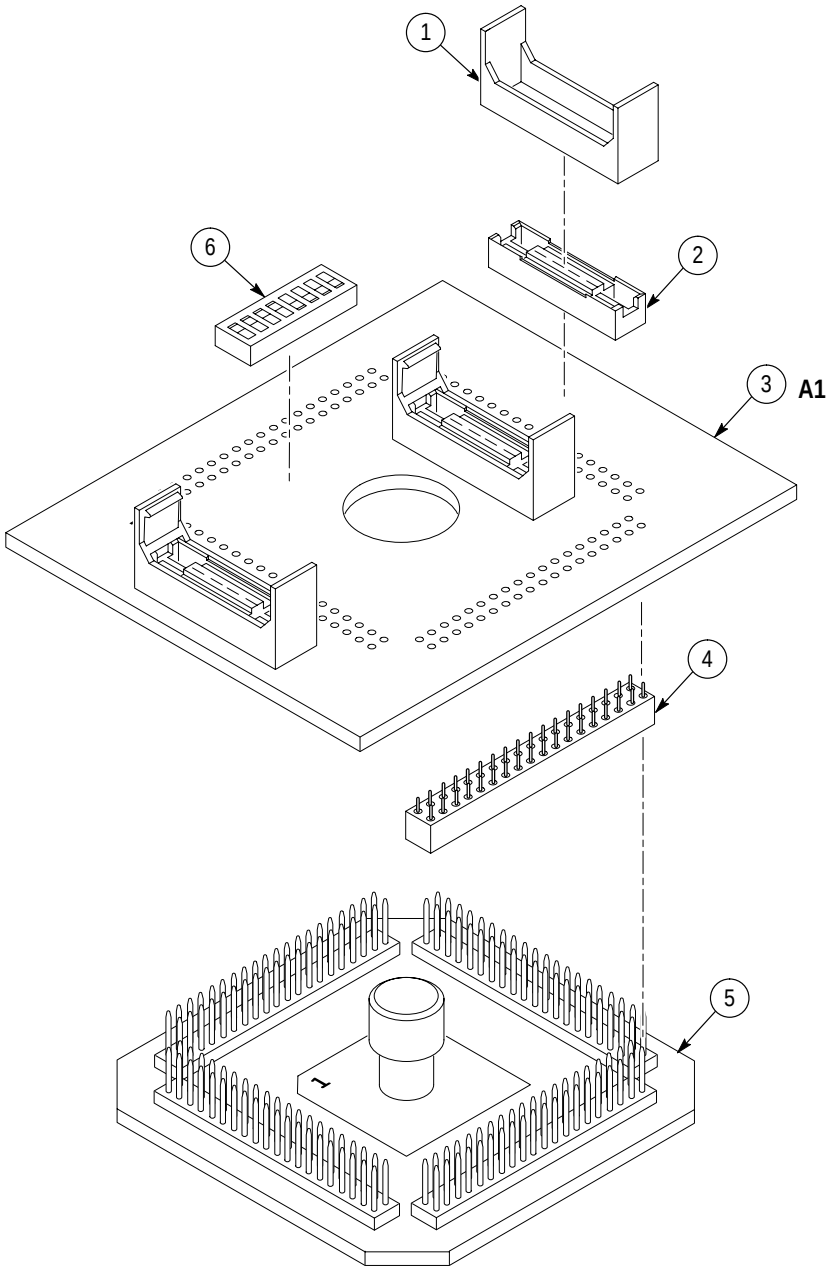


Figure 1: PowerPC MPC505 probe adapter exploded view

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DIAGRAMS AND CIRCUIT BOARD ILLUSTRATION

SYMBOLS

Graphic symbol and class designation letters are based on ANSI Y32.14, 1973 in terms of positive logic. logic symbols are depicted according to the manufacturer's data book information (not according to function).

Letter symbols for quantities used in electrical science and electrical engineering are based on ANSI Y10.5, 1968.

Drafting practices, line conventions, and lettering conform to ANSI Y14.12, 1966 and ANSI Y14.2, 1973.

Abbreviations are based on ANSI Y1.1, 1972.

You can inquire about these ANSI standards by contacting:

American National Standard Institute
1430 Broadway
New York, New York 10018

COMPONENT VALUES

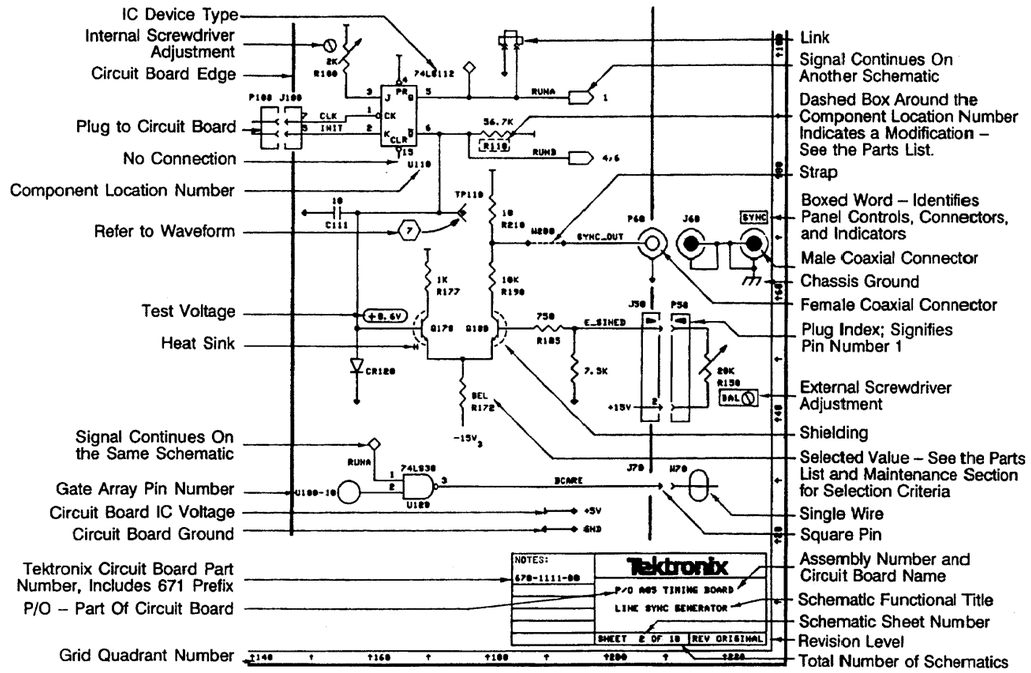
Electrical components shown on the diagram are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF)
Values less than one are in microfarads (μF)

Resistors = Ohms (Ω)

ACTIVE-LOW SIGNAL INDICTORS

A common convention used for indicating an active-low signal (a signal performing its intended function when it is in a low state) is an overbar, as shown in the signal name $\overline{\text{RESET}}$. The overbar may be used in this manual whenever a reference is given to an active-low signal. However, the same active-low signal. However, the same active-low signal is indicated on the schematic with a tilde (~), or a slash (*) following the signal name (e.g., RESET ‘ or RESET*).



The information and special symbols below may appear in this manual.

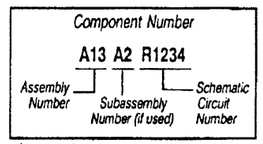
ASSEMBLY NUMBERS

Each assembly in the instrument is assigned as assembly number e.g., A5). The assembly number appears in the title of each:

- schematic diagram (lower right corner)
- circuit board component location look up table (when shown).
- schematic or circuit board component location look up table (when shown).

The Replaceable Electrical Parts list is arranged by assemblies in numerical order. The components are listed alphabetically by component location numbers. Look at the following example to see how to construct a component number.

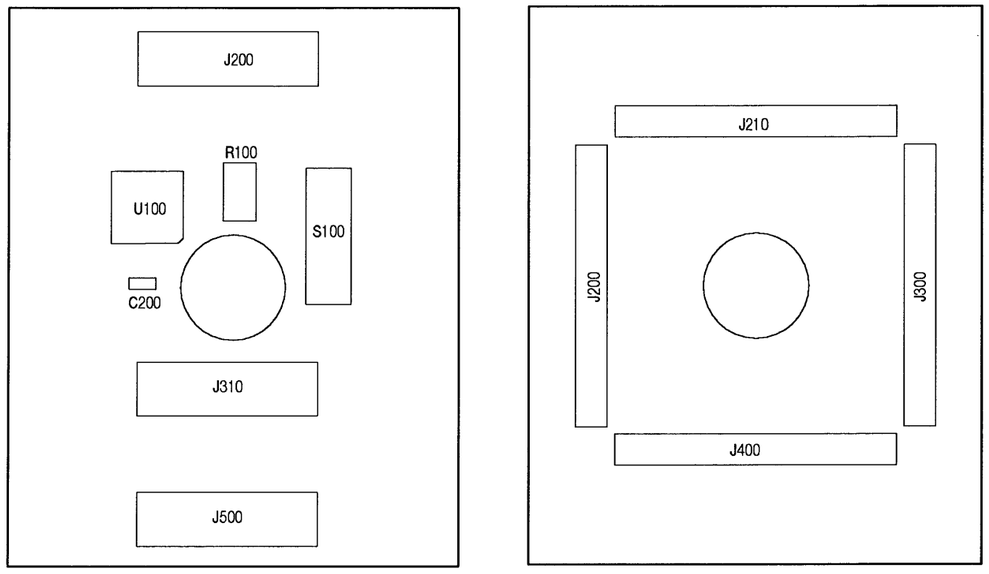
COMPONENT NUMBER EXAMPLE



Chassis mounted components have no Assembly Number prefix – see end of Replaceable Parts List.

GRID COORDINATES

The schematic diagram(s) and circuit board component location illustration both have grids. A look up table (when shown) provides grid coordinates for ease of locating components. There may be two tables for each assembly: one for the circuit board component location illustration and one for the schematic diagram(s).



Front

Back

A01: PowerPC MPC505 circuit board component locations

CONTROL<28..0>

DATA<32..0>

ADDRESS<29..0>

J210
FM40_B

J300
FM40_B

J400
FM40 B

J320
FM40_B

J310
FM38GND5LATCH

J500
FM38GND5LATCH

J200
FM38GND5LATCH

MICTOR A

MICTOR D

MICTOR C

S100

U100
PAL_LV22V107JC
PAL_IMAGE

C200
0.1UF

RES_15PKMOD
R100

NO_CS*

PROJECT_NAME=TMS550

BOARD_NAME=MPC505 160 QFP PROBE ADAPTER

UC, PAL LOGIC AND MICTOR CONNECTORS A01

1
OF: 1